

An AP210-based Repository for Collaborative Electronics Engineering

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Outline

AP210-based Environment - JPL/NASA Phase 1

- Ancillary Information Problem
- Phase 1 Scope (work-in-progress)
- Collaboration
- Expected Benefits

Other Potential AP210 Applications:

Chip Package Design & Analysis - Shinko Phase 1, 2

- Phase 1 Accomplishments

References & Nomenclature

Development of Advanced Collaborative Engineering Environments (CEEs)

Phase 1: CEE-based PWB Stackup Design Tool



Current engineering computing environments can be characterized as largely disjoint sets of tools that exchange information via labor-intensive processes. While some progress has been made, a good deal of engineering knowledge is not available in effective electronic forms, and interoperability among engineering processes is less than optimum.



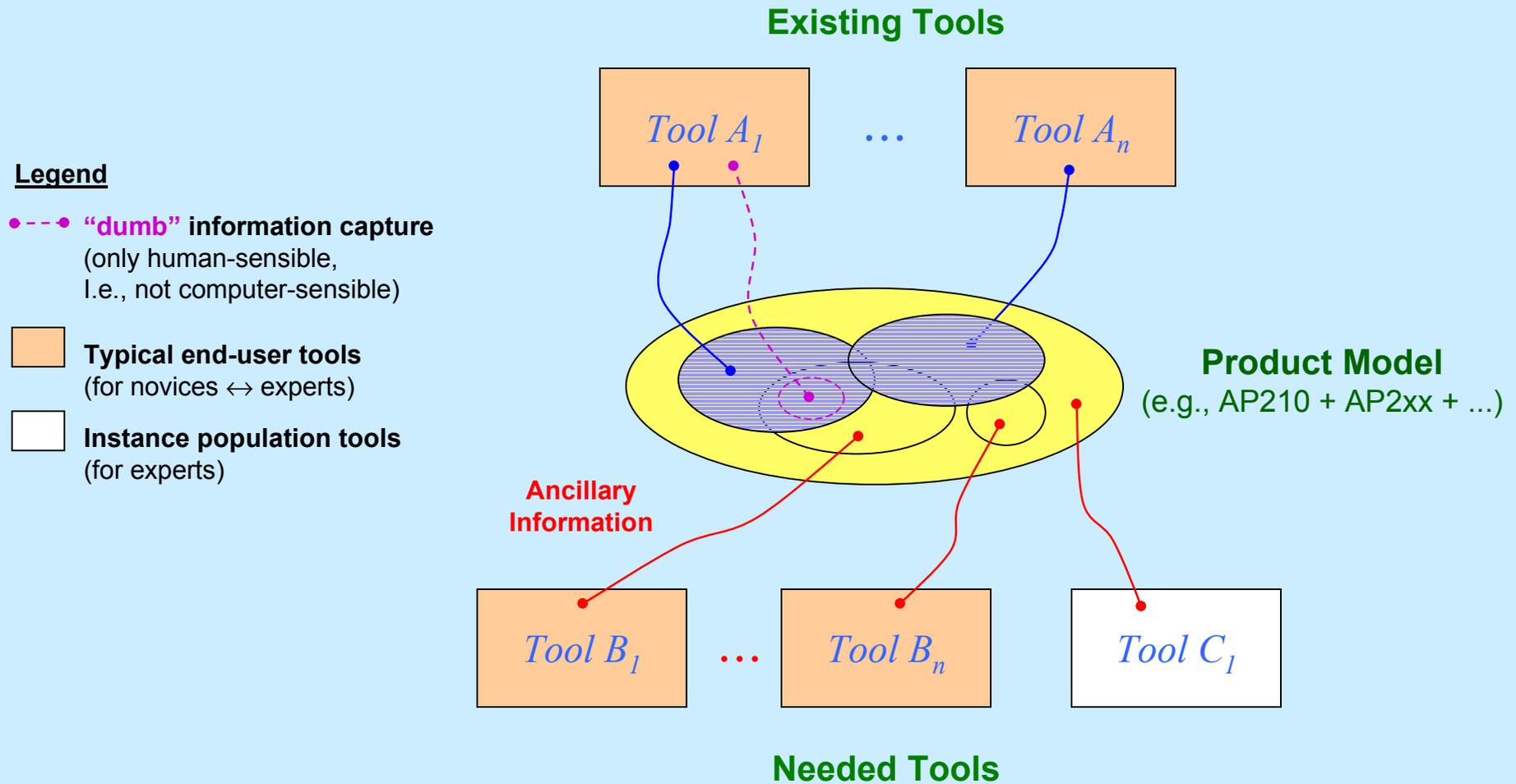
For example, today engineers still often manually add numerous notes and sketches to CAD drawings. In spite of being in an electronic form, these notes and sketches are in a relatively low-level representation that is not easily processed by downstream tools. They are primarily intended for human consumption. These items typically require manual intervention and re-creation downstream, resulting in increased labor efforts and transcriptions errors.

Thus, there is a great need to capture the higher level concepts behind these items (e.g., PWB stackup design intent) in semantically rich knowledge containers. Associativity with other types of information is also needed (e.g., other rich objects that exist in some current CAD tools). This Phase 1 effort is aimed at a) developing a general methodology and computing framework for capturing this ancillary information, and b) implementing a prototype PWB stackup tool in this framework to demonstrate this approach.

Phase 1 helps JPL/NASA move along the roadmap defined in Phase 0 to achieve a next-generation collaborative engineering environment. The target environment will leverage advances in engineering information technology, including standards like STEP, to achieve fine-grain, modular interoperability among design objects and related tools. Techniques based on efforts including Georgia Tech CAD-CAE integration research will be applied and enhanced, and new approaches will be developed as needed. The target outcome is a virtual collaborative engineering environment which increases product life cycle effectiveness by an order of magnitude or greater.

This presentation overviews work-in-progress for Phase 1.

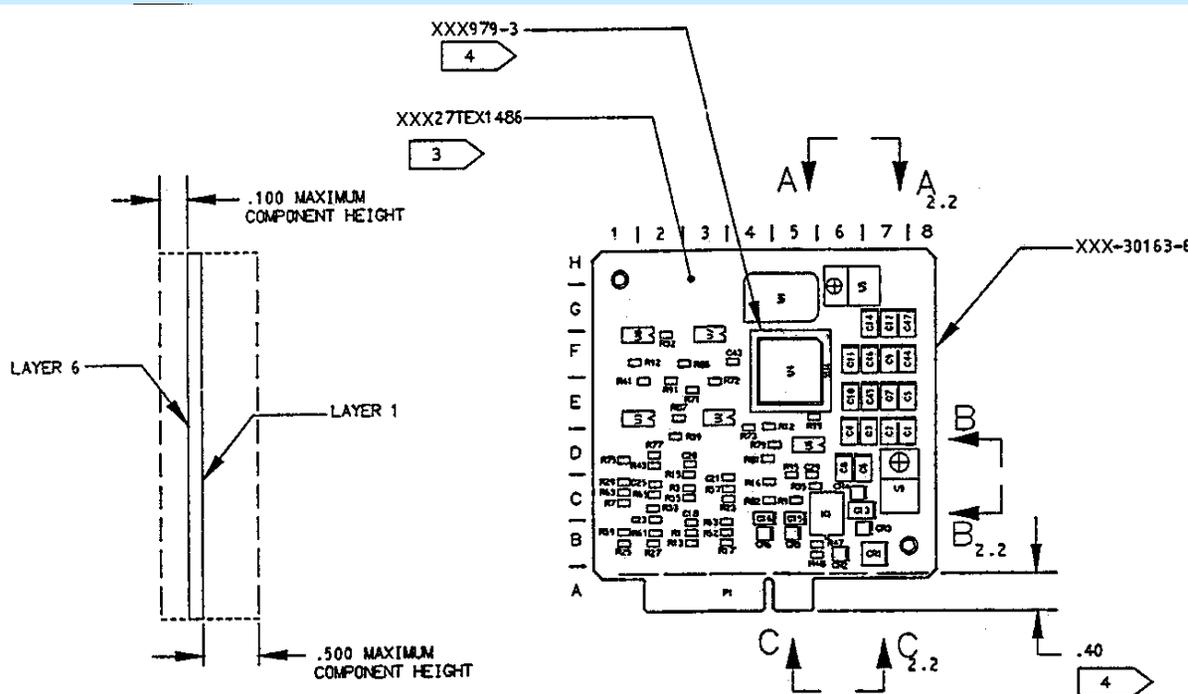
Problem: Insufficient Information Capture



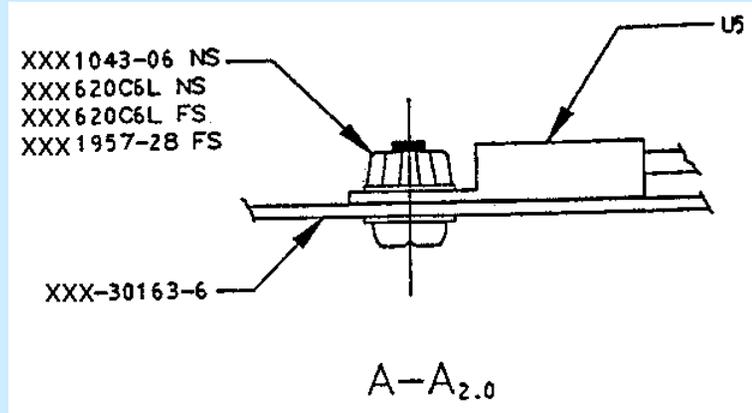
Example PWA Ancillary Information

PWA = printed wiring assembly
 PWB = printed wiring board

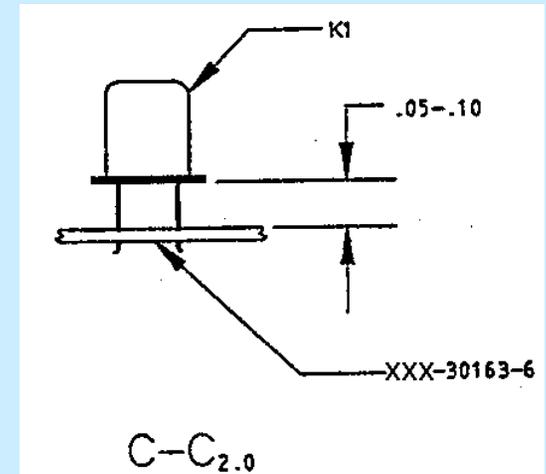
Maximum Height Restrictions



Conformal Coating Restrictions

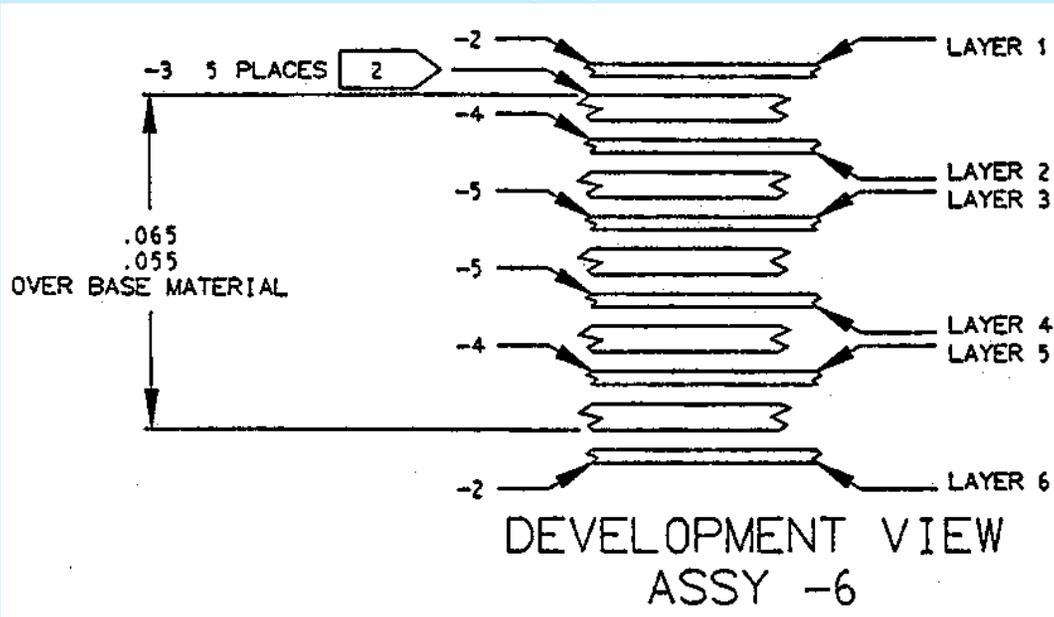


Component Assembly Instructions

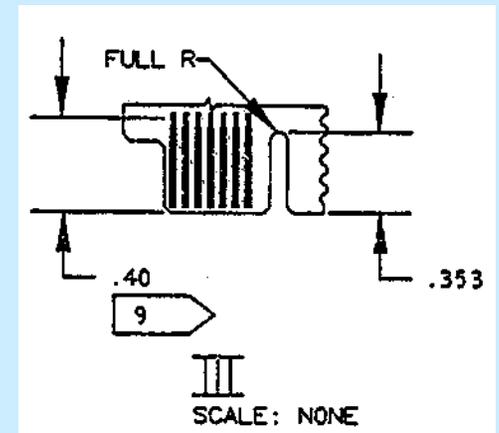


Example PWB Ancillary Information

Stackup Specs



Outline Detail



Stackup Notes

NOTES:

- 1 MANUFACTURE USING CONDUCTOR PATTERN PER TABLE II OF DRAWING. SEE TABLES I AND III FOR HOLE CODE TABLE.
- 2 MINIMUM DIELECTRIC SPACING IS .0035 INCH. A MINIMUM OF TWO SHEETS OF GLASS CLOTH IS REQUIRED.
- 3 COPPER FOIL PER XXX325, FORM C1, ANY GRADE. EXTERNAL VENDORS SHALL USE COPPER FOIL PER XXX-10063, TYPE C, ANY GRADE, WEIGHT 1 OZ. COPPER IN THE FORM OF COPPER FOIL CLAD EPOXY/GLASS LAMINATED SHEETS OR COPPER FOIL IS ACCEPTABLE.
- 4 EPOXY/GLASS LAMINATED SHEETS PER XXX325, TYPE I, ANY CLASS, OR GLASS FABRIC REINFORCED B-STAGE EPOXY RESIN PER XXX-118, ANY TYPE, ANY FORM. EXTERNAL VENDORS SHALL USE EPOXY/GLASS LAMINATED SHEETS PER XXX-10063, TYPE GF, OR GLASS FABRIC REINFORCED B-STAGE EPOXY RESIN PER XXX-10063, TYPE PGF.

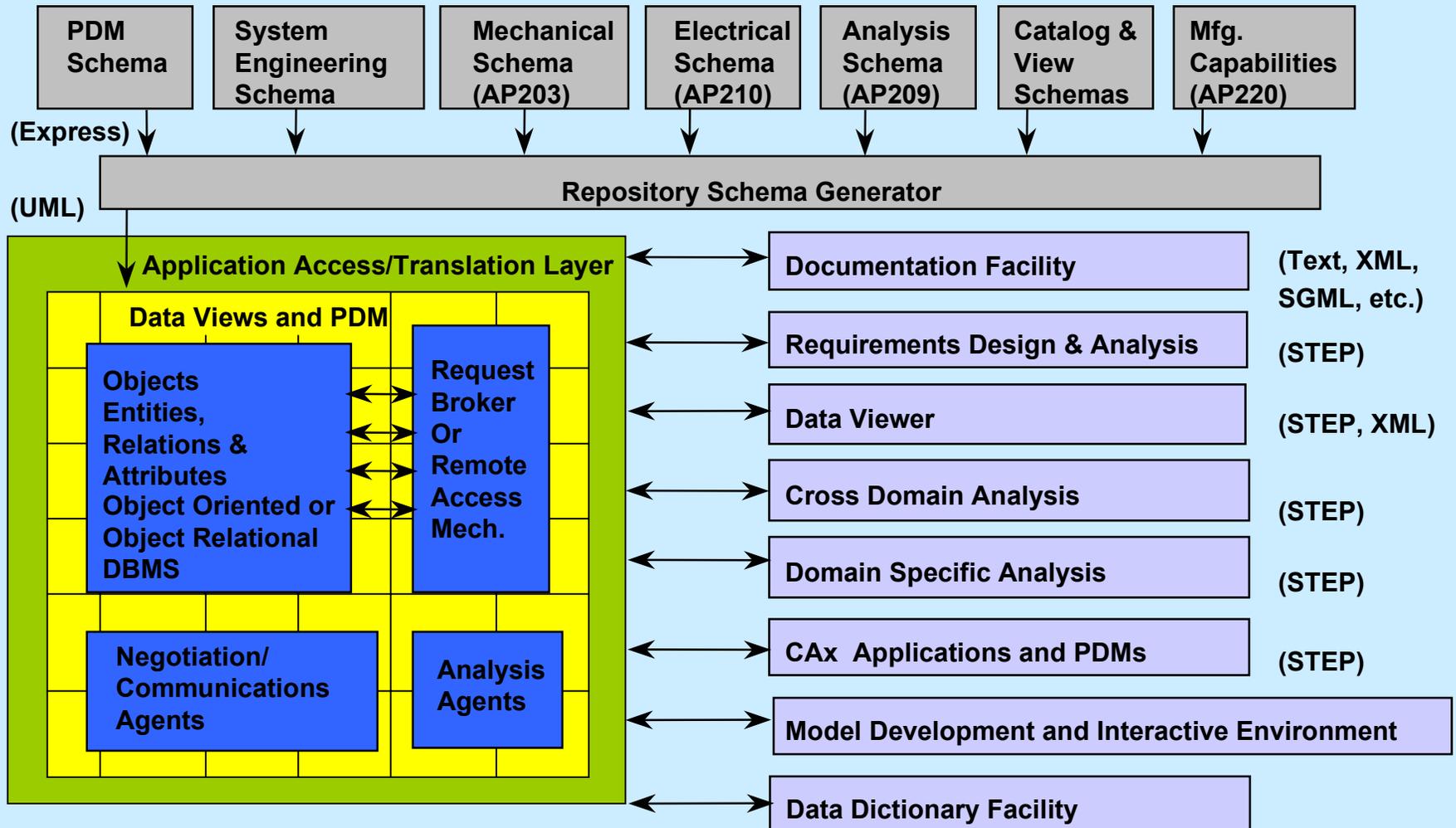
Current Situation (typical)

- ◆ CAx tools of diverse disciplines
- ◆ Each focuses on information subset (some overlap)
- ◆ Much ancillary information
 - Some captured as “dumb” notes & sketches in CAD
 - » Human-oriented, not computer-sensible
 - Much not captured at all
 - Lack of fine-grain explicit associativity
- ◆ Problems
 - Manually intensive transformations
 - Error-prone transcription / re-creation downstream
 - Little knowledge capture

Target Situation *(longer term)*

Collaborative Engineering Environment with Advanced Interoperability

Potential Standards-based Architecture (after G. Smith, Boeing)



Outline

AP210-based Environment - JPL/NASA Phase 1

- Ancillary Information Problem
- Phase 1 Scope (work-in-progress) 
 - » Background: ProAM/TIGER Projects, XAI
 - » Phase 1 Architectures
- Collaboration
- Expected Benefits

Other Potential AP210 Applications:

Chip Package Design & Analysis - Shinko Phase 1, 2

- Phase 1 Accomplishments

References & Nomenclature

- ◆ Initial step towards vision
- ◆ Capture of representative ancillary information
 - Focus: PWB stackup information
 - Extend Georgia Tech stackup tool (from ProAM)
 - STEP AP210 as information container structure
 - Develop & demonstrate method
- ◆ Initial steps (Phase 1): file-oriented
 - Use Metaphase as PDM capability
 - Manage files: ECAD file, MCAD file, Gerber file, stackup tool file (AP210 subset), ...
- ◆ Next steps (Phase 1+, 2):
Fine-grained interactive sharing (Accelis-type tools)

STEP AP 210

PWA/B Design Information

Physical

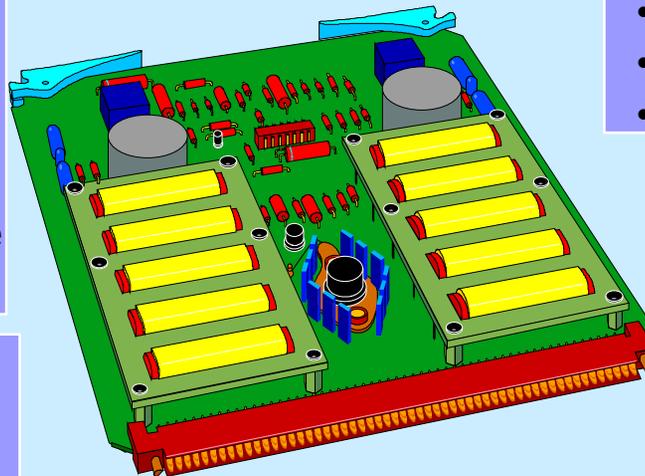
- Component Placement
- Bare Board Geometry
- Layout items
- Layers non-planar, conductive & non-conductive
- Material product

Geometry

- Geometrically Bounded 2-D Shape
- Wireframe with Topology
- Advanced BREP Solids
- Constructive Solid Geometry

Product Structure/Connectivity

- Functional
- Packaged



Part

- Functionality
- Termination
- Shape 2D, 3D
- Single Level Decomposition
- Material Product
- Characteristics

Configuration Mgmt

- Identification
- Authority
- Effectivity
- Control
- Requirement Traceability
- Analytical Model
- Document References

Requirements

- Design
- Allocation
- Constraints
- Interface

Technology

- Fabrication Design Rules
- Product Design Rules



ProAM Design-Analysis Integration

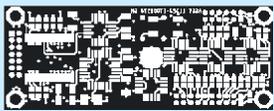
Electronic Packaging Examples: PWA/B

Completed
6/99

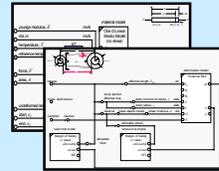
Design Tools

ECAD Tools

Mentor Graphics,
Accel*



STEP AP210[‡]
GenCAM**,
PDFI*



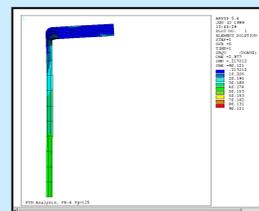
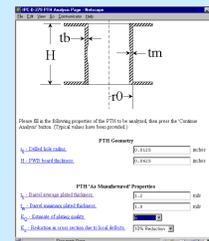
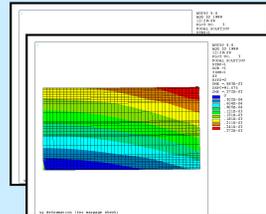
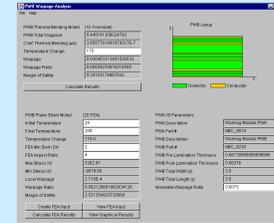
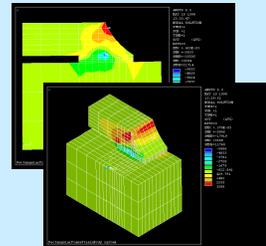
Modular, Reusable Template Libraries

Analysis Modules (CBAMs) of Diverse Behavior & Fidelity

XaiTools
PWA-B

Analysis Tools
General Math
Mathematica

FEA Ansys



Solder Joint
Deformation* 1D,
2D,
3D

PWB
Warpage 1D,
2D

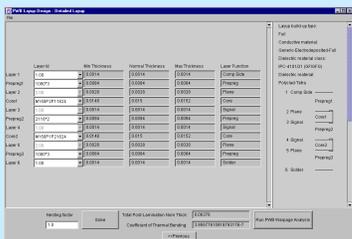
PTH
Deformation
& Fatigue** 1D,
2D

Analyzable Product Model

XaiTools
PWA-B



PWB Stackup Tool XaiTools PWA-B



Laminates DB



Materials DB

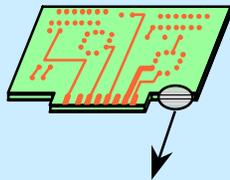


[‡] AP210 DIS WD1.7 * = Item not yet available in toolkit (all others have working examples) ** = Item available via U-Engineer.com

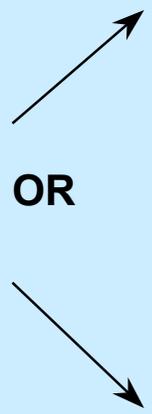
Overview of PWB Stackup Design

Fabrication engineer designs PWB stackup details

Stackup Specs - PWA/B Designer

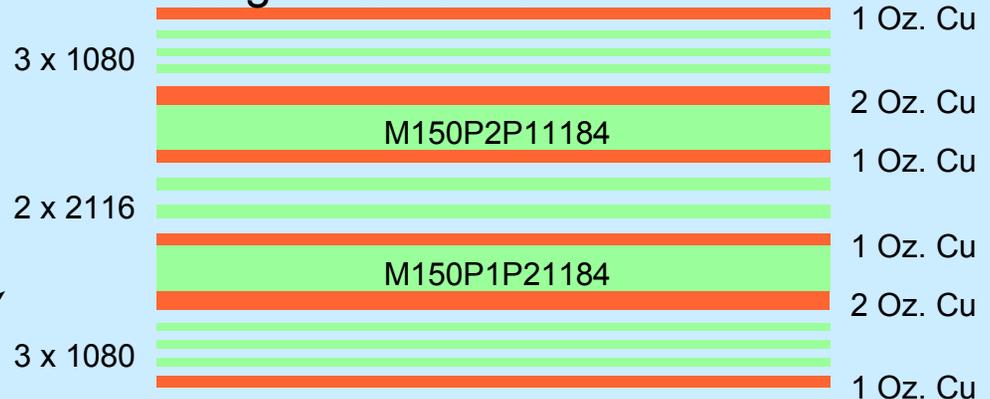


	component	
		Layer 1: 1 Oz. Cu Foil
		Epoxy Glass GF/ PGF
	plane	
		Layer 2: 2 Oz. Cu Foil
		Epoxy Glass GF/ PGF
	signal	
.065		Layer 3: 1 Oz. Cu Foil
.055		Epoxy Glass GF/ PGF
over	signal	
base		Epoxy Glass GF/ PGF
material	plane	
		Layer 4: 1 Oz. Cu Foil
		Epoxy Glass GF/ PGF
	plane	
		Layer 5: 2 Oz. Cu Foil
		Epoxy Glass GF/ PGF
	solder	
		Layer 6: 1 Oz. Cu Foil



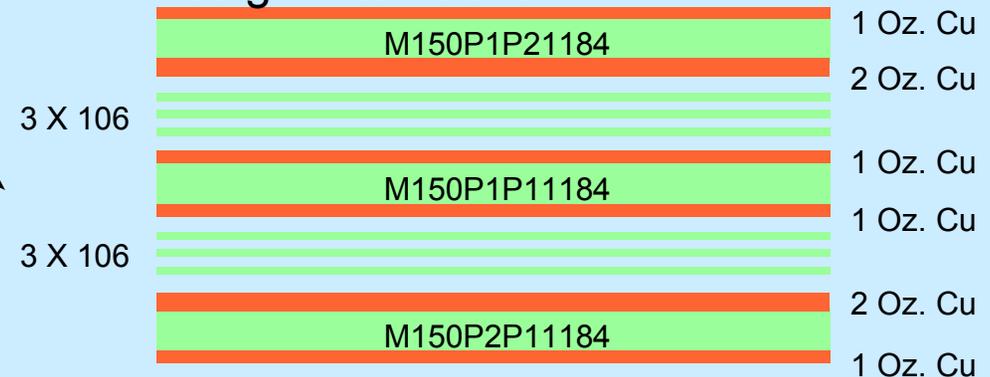
Stackup Design - PWB Fabricator

Design Alternative 1



...

Design Alternative n





Post-Lamination Thickness Calculation

Before: Typical Manual Worksheet
(as much as 1 hour engr. time)

Multilayer - Shear / Print / Lay Up Instructions

Panel Size 16 X 18 No. Up 6 Etx # 14718 W/O # 55 689-00

Thickness Measure: Overall/NiAu Over Base Lam. X Minimum Dielectric .0035

Finished Thickness: Minimum .026 Nominal .093 Maximum .100

Laminated Thickness: Minimum .090 Nominal .096 Maximum .102

Material Used: Tetra Polyimide Copper Used: Double Treat X

Tetra II Other HTE X

Stamp Work Order # On Lightest Weight Side:

Clip 1 Corner(s) Of: _____ Mat'l. _____

* 012 12-29-95 _____ Mat'l. _____

* 029 _____ Mat'l. _____

* 010 _____ Mat'l. _____

* 029 _____ Mat'l. _____

* 012 _____ Mat'l. _____

* 098 ORL _____ Mat'l. _____

Expose _____ Ounce Side _____

Print 3 Panels Of Layers 2+3 On .028 P/1

Print 3 Panels Of Layers 4+5 On .028 P/1

Print _____ Panels Of Layers _____ On _____

Expose _____ Ounce Side _____

Layer No: Material

0. 1 oz Cu Comp

1-1080
1-2116
1-1080

2. 028 P/1 PLANE

3. 1-1080 Sig

4. 1-2116 Sig

5. 028 P/1 PLANE

6. 1-1080 Sig

7. 1-2116 Sig

8. 1 oz Cu S/W

9. _____

10. _____

11. _____

12. core .056

.0036

13. 3 X .005 .016

.0315

14. _____

15. _____

16. _____

SPAL INSTRUCTIONS:

After: Tool-Aided Design (ProAM)

$$post_lamination_thickness = \sum_{i=1}^n nested_thickness_i$$

$$nested_thickness_{prepreg_set} = \sum_{i=1}^p k_n t_{sf_i} - resin_to_fill$$

$$\alpha_B = C_1 \frac{\sum t_i \alpha_i y_i}{(t^2/2)} + C_2 \frac{\sum |t_i \alpha_i y_i|}{(t^2/2)} + C_3$$

PWB Layout Design : Detailed Layout

Layer Id	Min Thickness	Normal Thickness	Max Thickness	Layer Function
Layer 1	2.00	0.0028	0.0028	Comp Side
Core1	L210150C2/C2AC	0.0125	0.015	Core
Layer 2	2.00	0.0028	0.0028	Signal
Prepreg1	1080*3	0.0060	0.0069	Prepreg
Layer 3	2.00	0.0028	0.0028	Signal
Core2	L210150C2/C2AC	0.0125	0.015	Core
Layer 4	2.00	0.0028	0.0028	Signal
Prepreg2	1080*3	0.0060	0.0069	Prepreg
Layer 5	2.00	0.0028	0.0028	Plane
Core3	L210150C2/C2AC	0.0125	0.015	Core
Layer 6	2.00	0.0028	0.0028	Plane
Prepreg3	1080*3	0.0060	0.0069	Prepreg
Layer 7	2.00	0.0028	0.0028	Signal
Core4	L210150C2/C2AC	0.0125	0.015	Core
Layer 8	2.00	0.0028	0.0028	Signal
Prepreg4	1080*3	0.0060	0.0069	Prepreg
Layer 9	2.00	0.0028	0.0028	Signal
Core5	L210150C2/C2AC	0.0125	0.015	Core
Layer 10	2.00	0.0028	0.0028	Solder

Nesting factor: 1.0 Solve

Total Post-Lamination Nom Thick: 0.11715999999999999

Coefficient of Thermal Bending: 3.9064225924153626E-7

Run PWB Warp

<<Previous exit

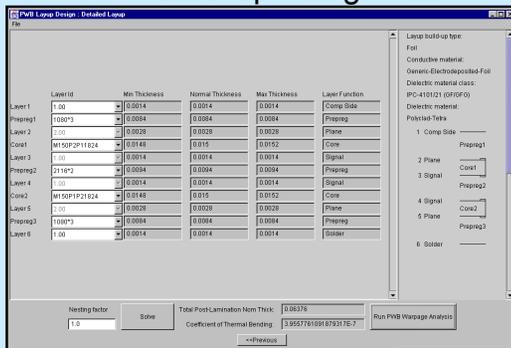


Iterative Design & Analysis

PWB Stackup Design & Warpage Analysis

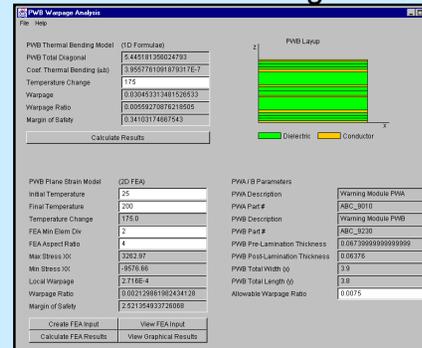
(TIGER extensions)

PWB Stackup Design Tool



Layup Re-design

1D Thermal Bending Model

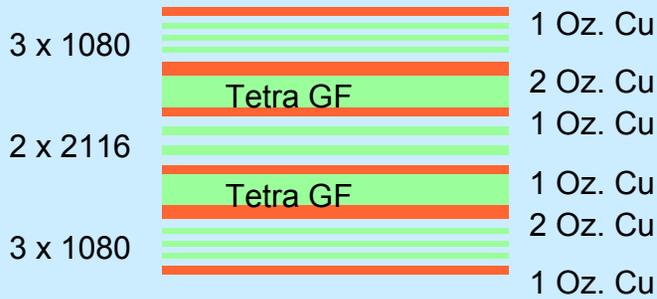


Quick Formula-based Check

$$\delta = \frac{\alpha_b L^2 \Delta T}{t}$$

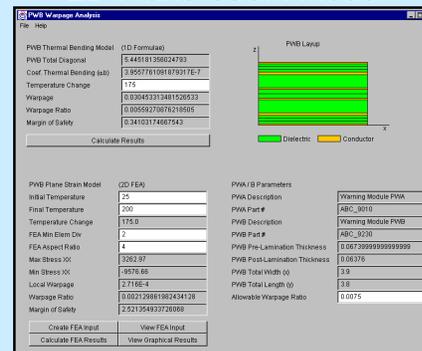
$$\alpha_b = \frac{\sum w_i \alpha_i y_i}{t / 2 \sum w_i}$$

Analyzable Product Model

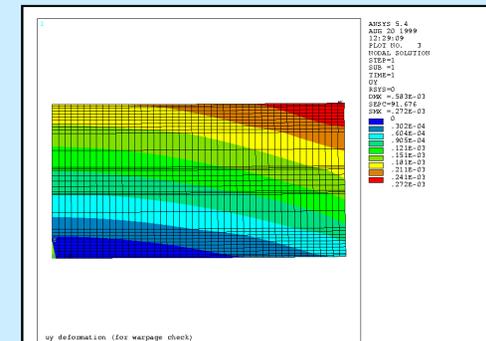


PWB Warpage Modules

2D Plane Strain Model



Detailed FEA Check

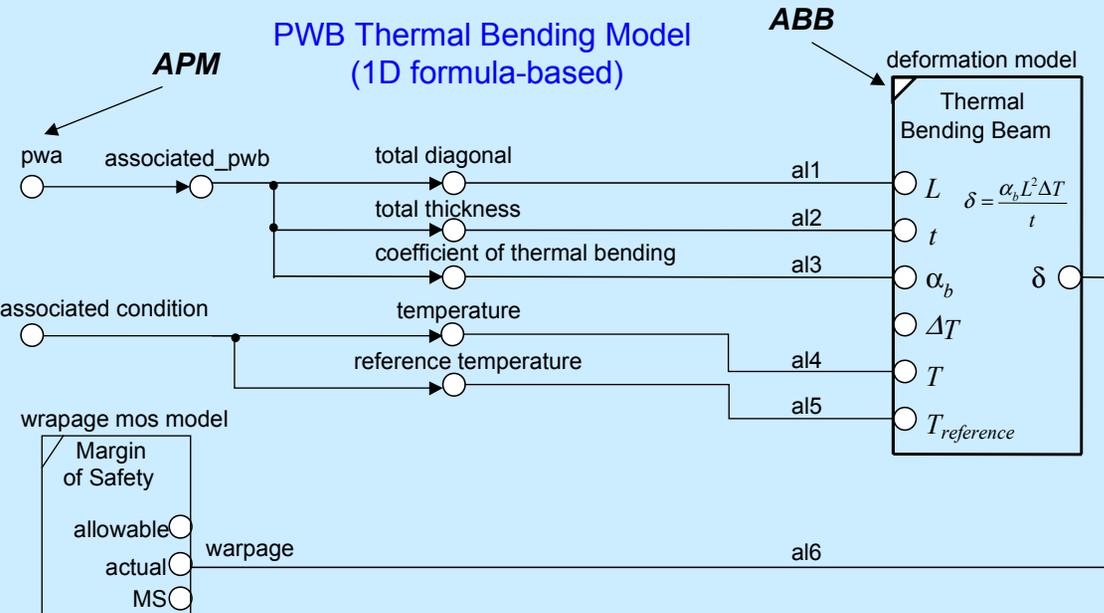




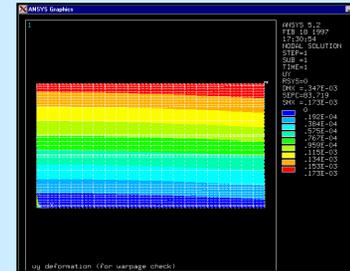
PWB Warpage Modules

a.k.a. CBAMs: COB-based analysis templates

PWB Thermal Bending Model
(1D formula-based)

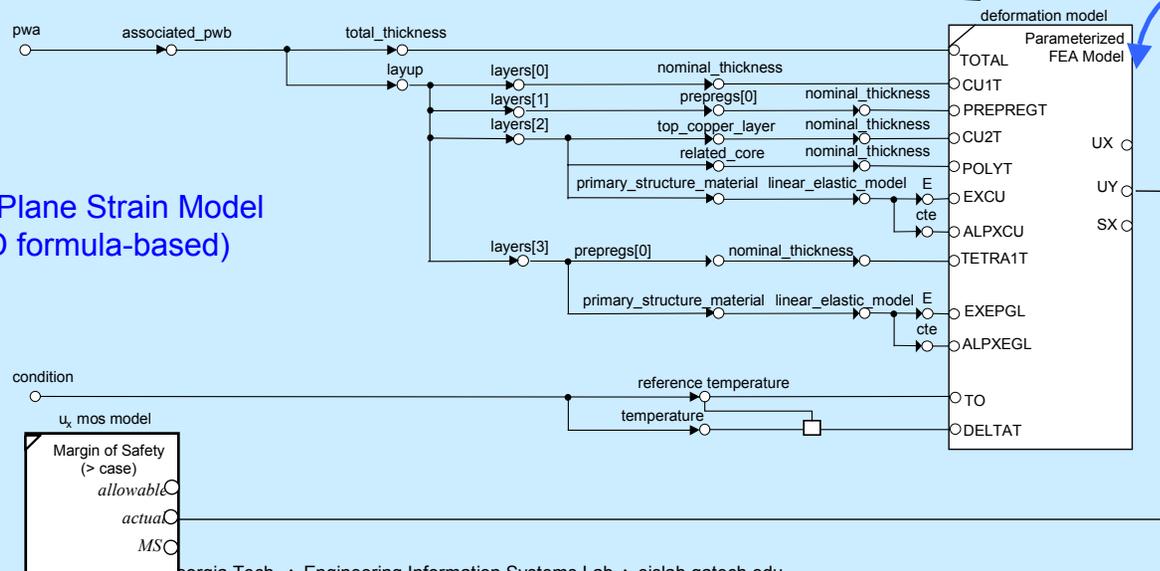


SMM



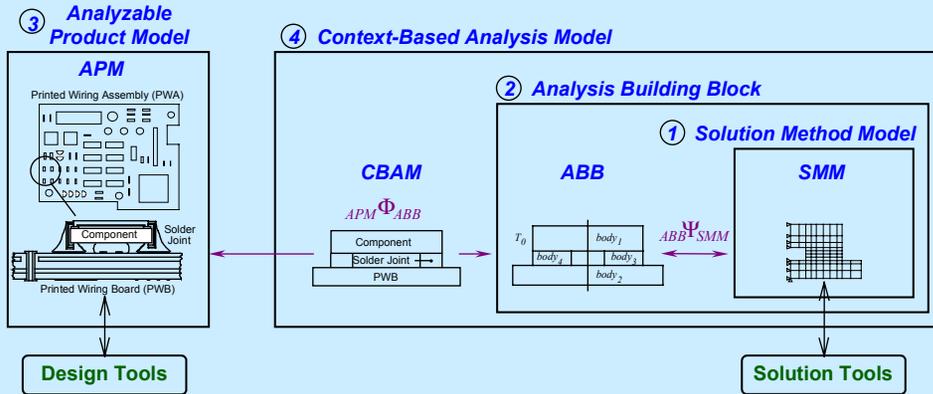
ABB

PWB Plane Strain Model
(2D formula-based)

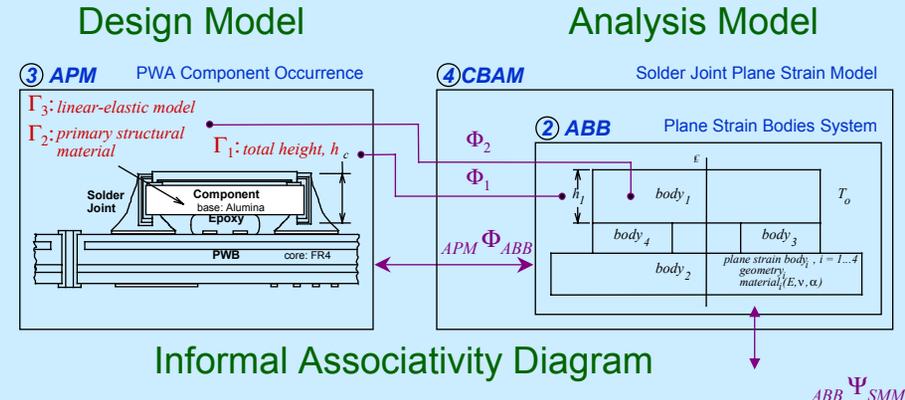


X-Analysis Integration Techniques

a. Multi-Representation Architecture (MRA)

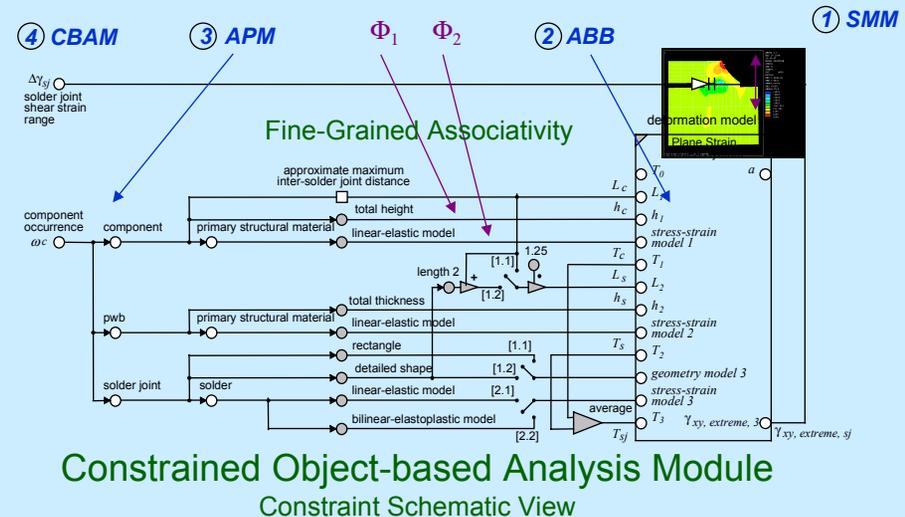
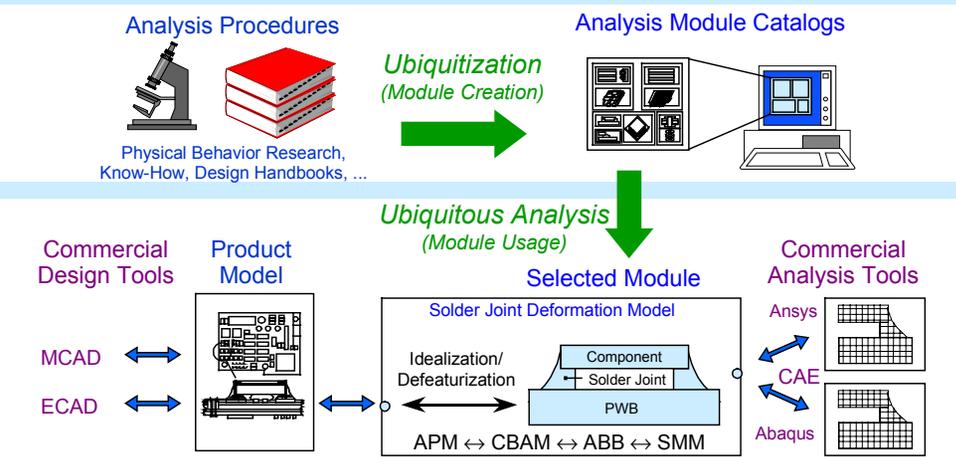


b. Explicit Design-Analysis Associativity



Informal Associativity Diagram

c. Analysis Module Creation Methodology

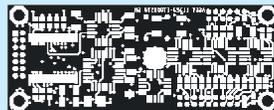


Constrained Object-based Analysis Module Constraint Schematic View

Design Tools

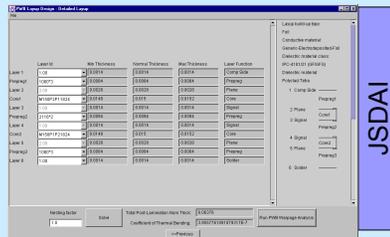
ECAD Tools

Mentor Graphics,
Cadence



PWB Stackup Tool

XaiTools PWA-B



Laminates Library Materials Library

Instance Browser/Editor

AP210 Viewer,
STEP-Book AP210,
SDAI-Edit, ...



Native files

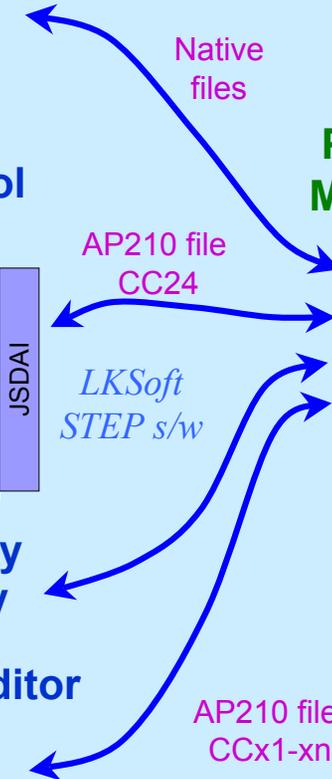
Product Knowledge Management System



AP210 file
CC24

LKSoft
STEP s/w

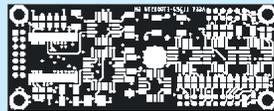
AP210 file
CCx1-xn



Design Tools

ECAD Tools

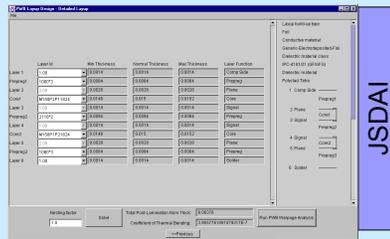
Mentor Graphics, Cadence



Other Tools

PWB Stackup Tool

XaiTools PWA-B



Laminates Library Materials Library

Instance Browser/Editor

*AP210 Viewer,
STEP-Book AP210,
SDAI-Edit, ...*



Standards-Based
Coarse/Fine-Grained
Interoperability ↔

Engineering Middleware

Product Knowledge Management System

AP210
content

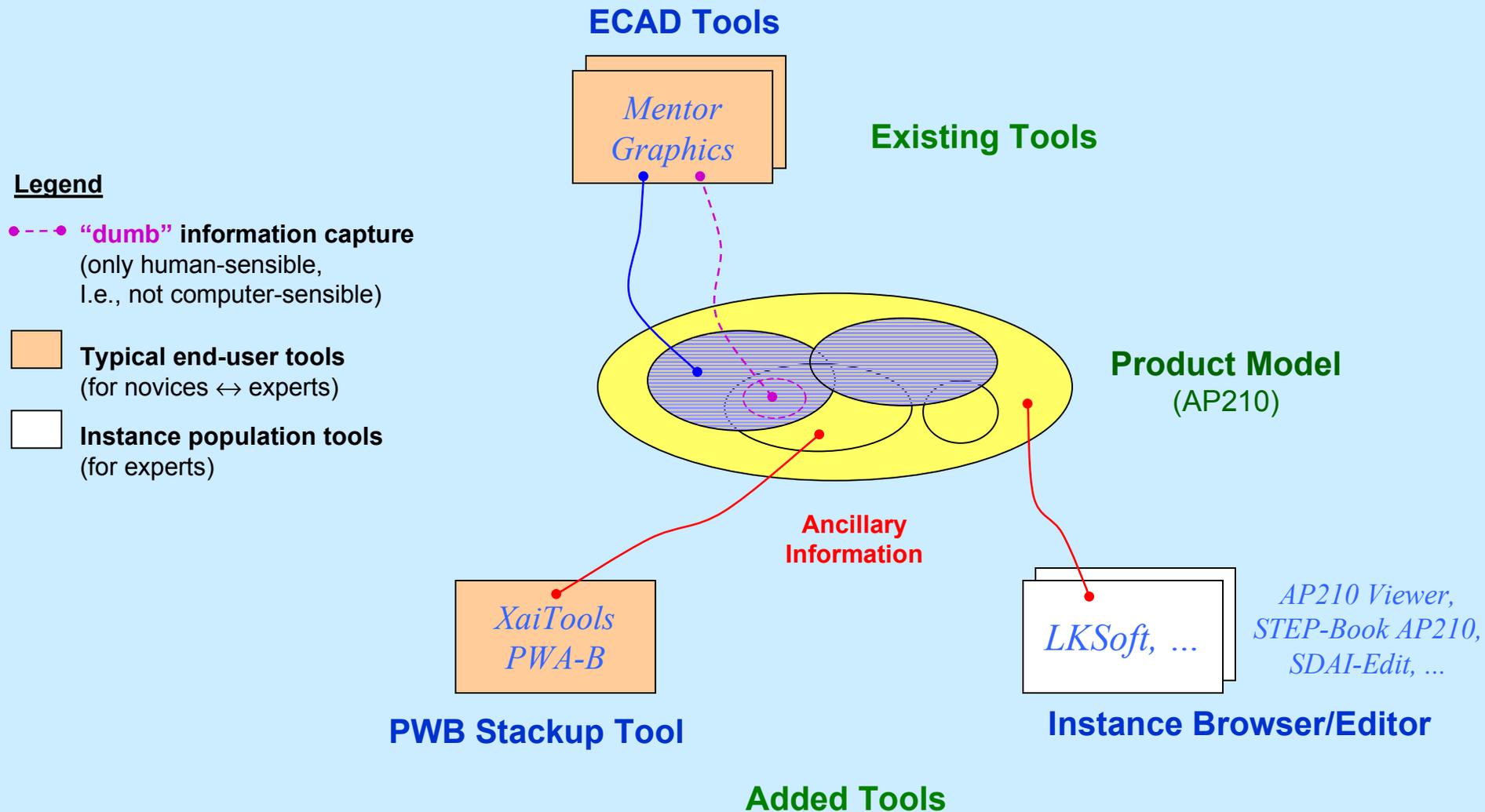
LKSoft
STEP s/w



J2EE-compliant
Web Application Server

Notes:
Accelis & Metaphase are SDRC products.

Phase 1 View



Collaboration

- ◆ JPL/NASA
 - Primary stakeholder, end users, tool experts
- ◆ Georgia Tech
 - Architecture/method, PWB stackup tool, XAI methods
- ◆ AP210 Implementers Forum
 - Common interests & techniques
 - Cooperative exchanges
- ◆ JPL/NASA suppliers
 - Software vendors

Expected Benefits: Phase 1

- ◆ STEP AP 210-based method
 - » Depth, extendibility
- ◆ Capture of ancillary information
 - Representative tool: PWB stackup design
 - » Graphics, automation
 - » Tangible end user benefits
 - » Technique illustration
 - “Better, faster, cheaper”
 - » Increased product model completeness
 - » Reduced downstream errors
 - » Increased automation
 - » Increased knowledge retention

Outline

AP210-based Environment - JPL/NASA Phase 1

- Ancillary Information Problem
- Phase 1 Scope (work-in-progress)
- Collaboration
- Expected Benefits

Other Potential AP210 Applications: 

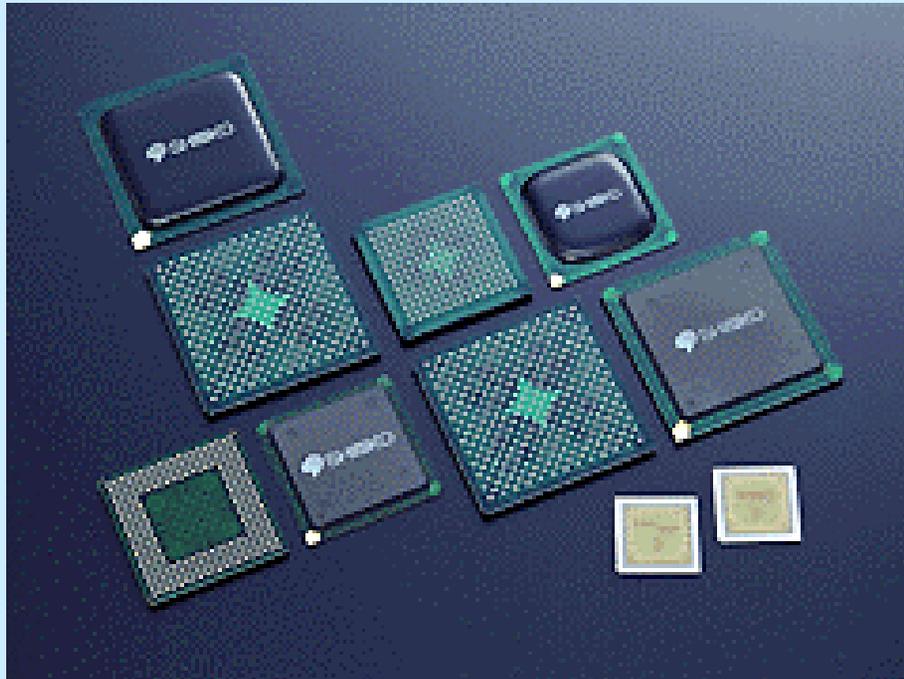
Chip Package Design & Analysis - Shinko Phase 1, 2

- Phase 1 Accomplishments

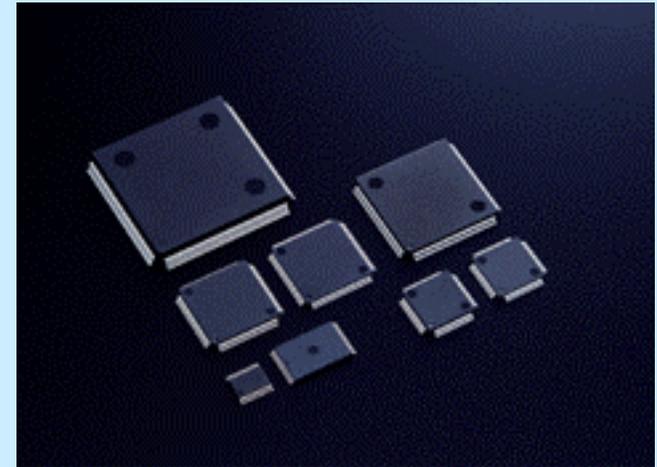
References & Nomenclature

Other Potential AP210 Applications

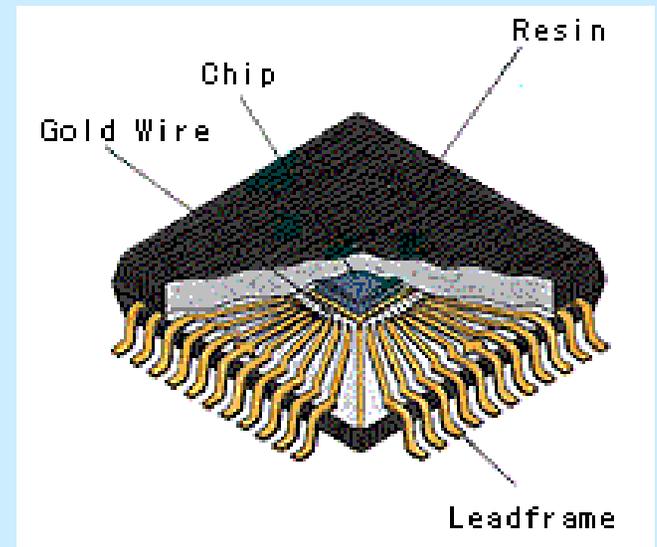
Chip Package Design & Analysis



Plastic Ball Grid Array (PBGA) Packages



Quad Flat Packs (QFPs)



Flexible High Diversity Design-Analysis Integration

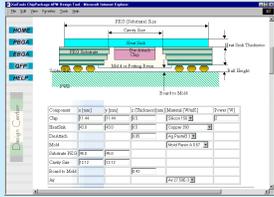
Electronic Packaging Examples: Chip Packages/Mounting

Shinko Electric Project: Phase 1 (completed 9/00)

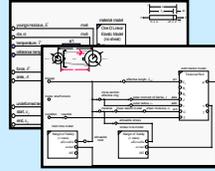
Design Tools

Prelim/APM Design Tool

XaiTools ChipPackage



PWB DB
Materials DB*



Modular, Reusable
Template Libraries

Analysis Modules (CBAMs)
of Diverse **Behavior** & **Fidelity**

Analysis Tools

General Math
Mathematica

FEA
Ansys

*XaiTools
ChipPackage*

Analyzable
Product Model



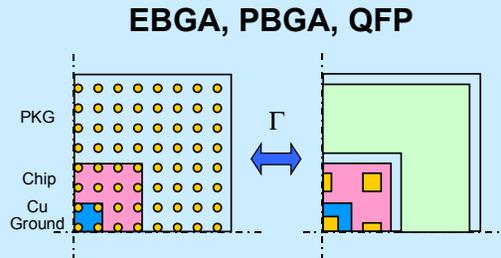
**Thermal
Resistance**

3D

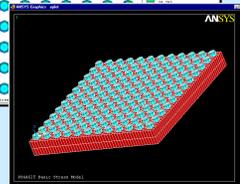
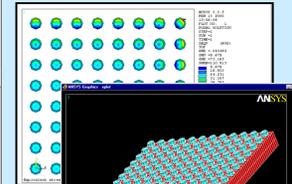
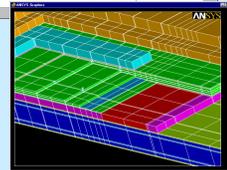
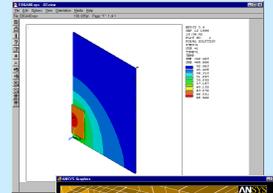
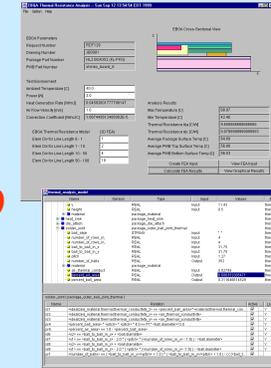
**Thermal
Stress**

Basic
3D**

Basic
Documentation
Automation



EBGA, PBGA, QFP



Authoring
MS Excel

** = Demonstration module

APM Design Tool

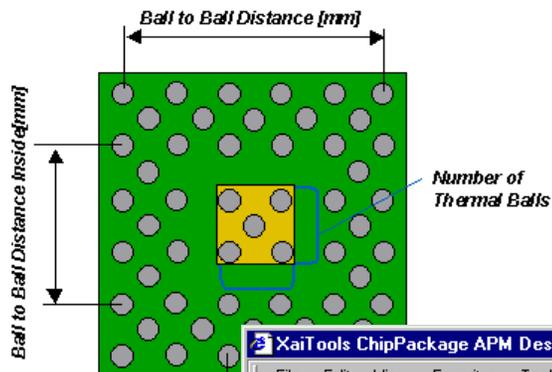
Preliminary Design of Packages - PBGA Screens

XaiTools ChipPackage APM Design Tool - Microsoft Internet Explorer

File Edit View Favorites Tools Help

HOME
PBGA
EBGA
QFP
HELP

Design Center



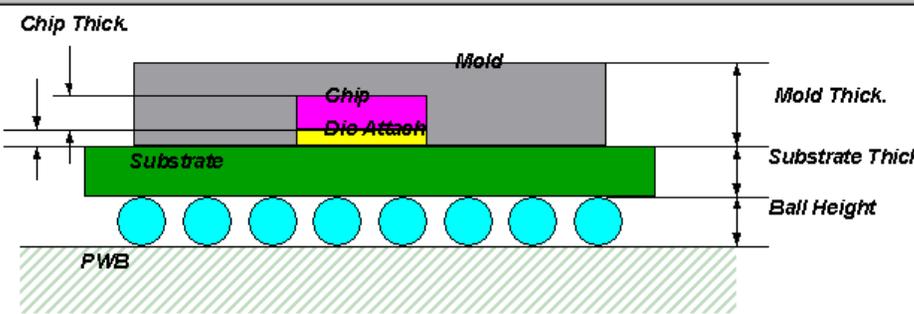
Number of Thermal Balls	Ball Pitch [mm]
41	1.27
Ball to Ball Distance X[mm]	Ball to Ball Distance Y [mm]
30.48	30.48
Ball to Ball Distance X [mm]	Ball to Ball Distance Y [mm]

XaiTools ChipPackage APM Design Tool - Microsoft Internet Explorer

File Edit View Favorites Tools Help

HOME
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Design Center

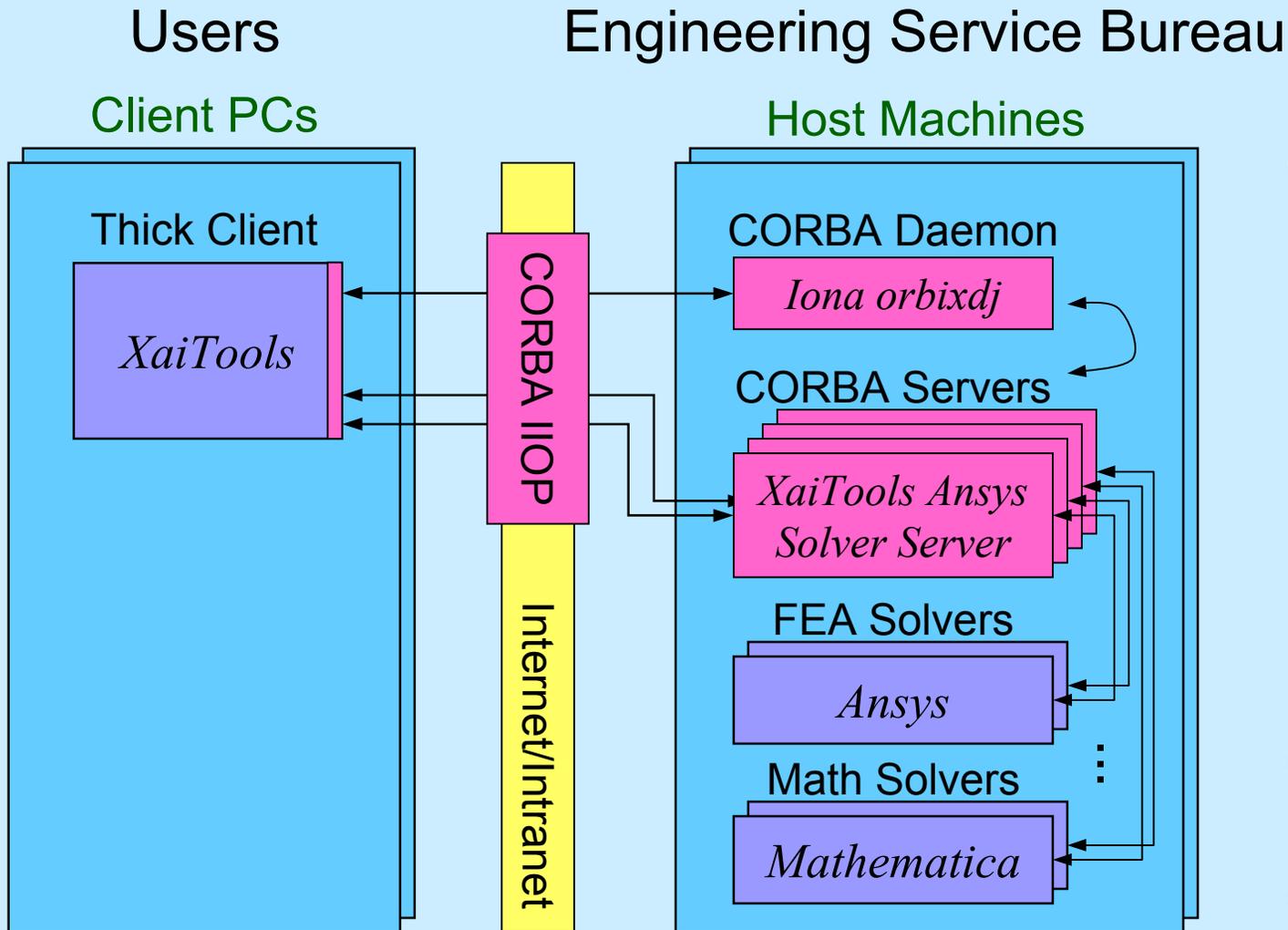


Component	x [mm]	y [mm]	z (Thickness)[mm]	Material [W/mK]	Power [W]
Chip	11.43	11.43	0.4	Silicon 150	2.0
Mold	30.0	30.0	1.2	Mold1 0.67	
DieAttach			0.05	Ag PasteC 3	
Substrate	35	35		BT-ResinA 0.2	
Air				Air 27.59E-3	

APM =
analyzable product model

Using Internet/Intranet-based Analysis Solvers

Thick Client Architecture



June'99-Present:

EIS Lab

- Regular internal use

U-Engineer.com

- Demo usage:

- US

- Japan

Nov.'00-Present:

Electronics Co.

- Began production usage (dept. Intranet)

Future:

Company Intranet

and/or

U-Engineer.com

(commercial)

- Other solvers

Pilot & Initial Production Usage Results

Product Model-Driven Analysis

- ◆ Reduced FEA modeling time > 10:1 (days/hours → minutes)
- ◆ Reduced simulation cycle > 75%

References

[1] Shinko 5/00 (in Koo, 2000)

[2] Shinko evaluation 10/12/00

<i>Analysis Model Creation Activity</i>	<i>With Traditional Practice</i>	<i>With VTMB Methodology*</i>	<i>Example</i>
Create initial FEA model (QFP cases)	8-12 hours	10-20 minutes	QFP208PIN
Create initial FEA model (EBGA cases)	6-8 hours	10-20 minutes	EBGA352PIN
Create initial FEA model (PBGA cases)	8-10 hours	10-20 minutes	PBGA256PIN
Create variant - small topology change	0.3-6 hours	(10-20 minutes) -	Moderate dimension change (e.g., EBGA 600 heat sink size variations)
Create variant - moderate topology change	(6-8 hours)-	(10-20 minutes) -	Add more features (e.g., increase number of EBGA steps)
Create variant - large topology change	(6-8 hours)+	(10-20 minutes)- or N/A	Add new types of features (e.g., add steps to EBGA outer edges)

- ◆ Enables greater analysis intensity → Better designs

Phase 1 Summary - Shinko Project

(Phase 2 is underway and evaluating usage of AP210)

Abstract Accepted for InterPACK'01
<http://www.asme.org/conf/ipack01/>

An Object-Oriented Internet-based Framework for Chip Package Thermal and Stress Simulation

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Abstract

Simulating the behavior of electronic chip packages like ball grid arrays (BGAs) is important to guide and verify their designs. Thermal resistance, thermomechanical stress, and electromagnetics impose some of the main challenges that package designers need to address. Yet because packages are composed of numerous materials and complex shapes, with current methods an analyst may spend hours to days creating simulations like finite element analysis (FEA) models.

This paper overviews work to reduce design cycle time by automating key aspects of FEA modeling and results documentation. The main objective has been automating FEA-based thermal resistance model creation for a variety of package styles: quad flat packs (QFPs), plastic BGAs (PBGAs), and enhanced BGAs (EBGAs). Pilot production tools embody analysis integration techniques that leverage rich product models and idealize them into FEA models. We have also demonstrated how the same rich product models can drive basic stress models with different idealizations.

In this framework, Internet standards like CORBA enable worldwide access to simulation solvers (e.g., Ansys and Mathematica). Automation and ease-of-use enable access by chip package designers and others who are not simulation specialists. Pilot industrial usage has shown that total simulation cycle time can be decreased 75%, while modeling time itself can be reduced 10:1 or more (from hours to minutes).

For Further Information ...

- ◆ EIS Lab web site: <http://eislabs.gatech.edu/>
 - Publications, project overviews, tools, etc.
 - See: Publications → DAI/XAI → Suggested Starting Points
X-Analysis Integration (XAI) Technology
<http://eislabs.gatech.edu/pubs/reports/EL002/>
- ◆ *XaiTools*[™] home page: <http://eislabs.gatech.edu/tools/XaiTools/>
- ◆ Pilot commercial ESB: <http://www.u-engineer.com/>
 - Internet-based self-serve analysis
 - Analysis module catalog for electronic packaging
 - Highly automated front-ends to general FEA & math tools

Nomenclature

Ψ	ABB-SMM transformation
Γ	idealization relation between design and analysis attributes
Φ	APM-ABB associativity linkage indicating usage of one or more Γ_i
ABB	analysis building block
AMCOM	U. S. Army Aviation and Missile Command
APM	analyzable product model
CAD	computer aided design
CAE	computer aided engineering
CBAM	context-based analysis model
COB	constrained object
COI	constrained object instance
COS	constrained object structure
CORBA	common ORB architecture
DAI	design-analysis integration
EIS	engineering information systems
ESB	engineering service bureau
FEA	finite element analysis
FTT	fixed topology template
GUI	graphical user interface
IOP	Internet inter-ORB protocol
MRA	multi-representation architecture
ORB	object request broker
OMG	Object Management Group, www.omg.com
PWA	printed wiring assembly (a PWB populated with components)
PWB	printed wiring board
SBD	simulation-based design
SBE	simulation-based engineering
SME	small-to-medium sized enterprise (small business)
SMM	solution method model
ProAM	Product Data-Driven Analysis in a Missile Supply Chain (ProAM) project (AMCOM)
PSI	Product Simulation Integration project (Boeing)
STEP	Standard for the Exchange of Product Model Data (ISO 10303).
VTMB	variable topology multi-body
XAI	X-analysis integration (X= design, mfg., etc.)
XCP	<i>XaiTools ChipPackage</i> [™]
XFW	<i>XaiTools FrameWork</i> [™]
XPWAB	<i>XaiTools PWA-B</i> [™]